Amendments to the Specification:

Please replace the paragraph beginning at page 34, line 5, with the following amended paragraph:

For example, in the case of VGA, the horizontal/vertical synchronous signal 24 and the clock signal are about 25 MHz. That is, in order to reproduce an image signal faithfully on a display, as a clock frequency for driving the horizontal scanning shift register 13 and the vertical scanning shift register 16, a frequency of at least 25 MHz, preferably about 50 MHz is required. Thus, all the D/A converter 14, buffers 17 and 18, and pixel matrix circuit 11 receiving the source signal and gate signal from the respective shift ~~resisters~~ registers 13 and 16 require a driving frequency of about 50 MHz (0.05 GHz).

Please replace the paragraph beginning at page 34, line 14, with the following amended paragraph:

Since the horizontal scanning oscillator 12 and the vertical scanning oscillator 15 for oscillating clock signals synchronous with the horizontal/vertical synchronous signal 24 to the respective shift ~~resisters~~ registers 13 and 16, require a driving frequency several times the shift ~~resisters~~ registers 13 and 16, there is a case where a high driving frequency of about 0.1 to 0.5 GHz is needed.

Please replace the paragraph beginning at page 36, line 20, with the following amended paragraph:

Thus, in Fig. 10A, the matrix circuit 11, shift ~~resisters~~ registers 13 and 16, D/A converter 14, buffers 17 and 18, and the like require the operating voltage of about 14 to 16 V. Although not shown in the block diagram of Fig. 10A, if a level shifter is provided in front of the buffer, the operating voltage thereof is also made about 14 to 16 V.